FYSE420 DIGITAL ELECTRONICS

Lecture 1

[1] **DIGITAL LOGIC CIRCUIT ANALYSIS & DESIGN**
Nelson, Nagle, Irvin, Carrol
ISBN 0-13-463894-8

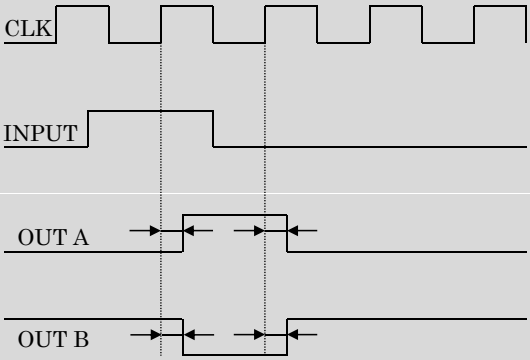
[2] **DIGITAL DESIGN**
Morris Mano
Fourth edition
ISBN 0-13-198924-3

[3] **Digital Design**
Principles and Practices
Fourth edition
Wakerly John F.
ISBN 0-13-186389-4

Asynchronous Sequential Logic

Introduction

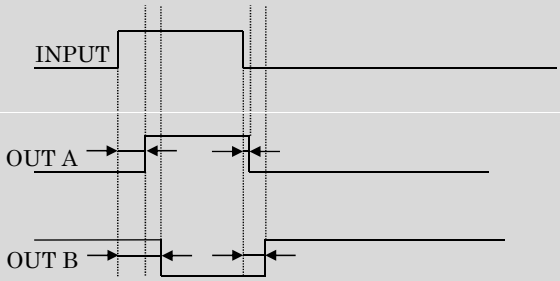
Synchronous sequential logic



The change of internal state occurs in response to the clock pulses.

Memory element : **clocked** filp-flops

Asynchronous sequential logic



The change of internal state occurs when there is change in the input variables.

Memory element : **unclocked** filp-flops or time-delay elements.

Asynchronous Sequential Logic

Introduction

Synchronous sequential logic

A properly designed system

↓

"No timing problems"

Needs a clock distribution

↓

Clock distribution takes a large amount of power in large VLSI chips

Asynchronous sequential logic

No clocked flip-flops **Feedback bath**

↓

Timing problems

↓

The design of asynchronous sequential circuits is difficult

Used when speed of operation is important

Fast response to the change of input variable

No clock distribution

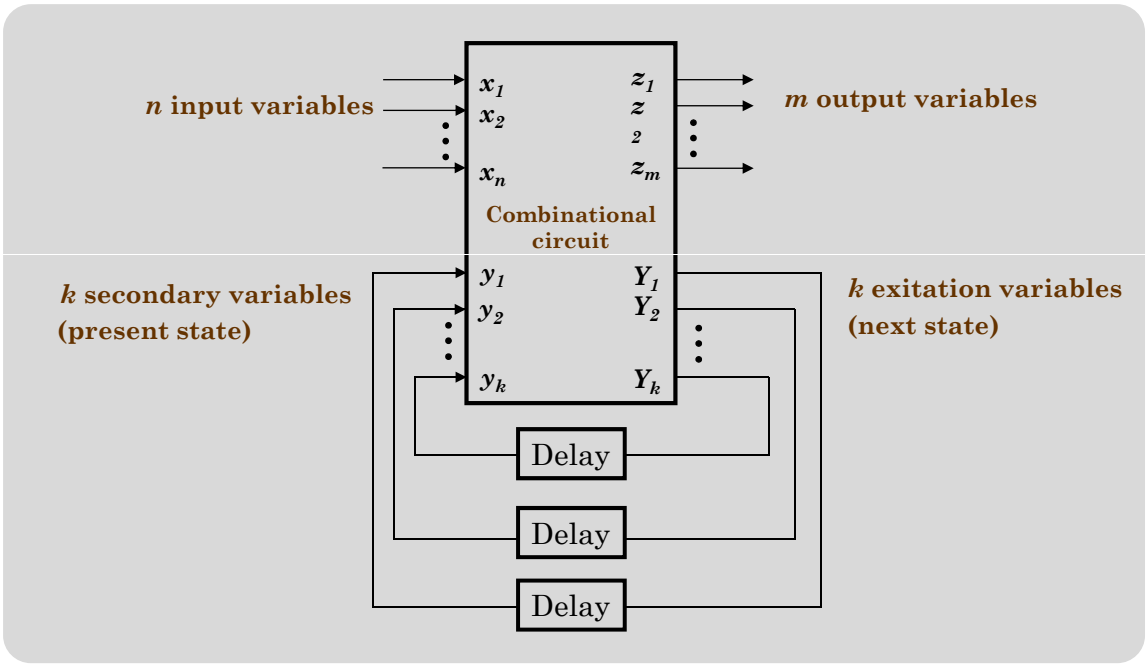
↓

Redused logic and power dissipation

Asynchronous Sequential Logic

Introduction

Block diagram of an asynchronous sequential circuit



Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

To ensure proper operation, circuits must be allowed to attain a stable state before the input is changed to a new value.

Because of delays in the wires and the gate circuits it is impossible to say which variable changes its state first when two or more input variables change at exactly same instant time.

Fundamental mode

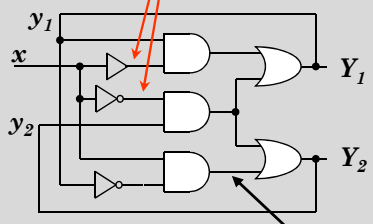
Input signals change one at a time and only when the circuit is in the stable state.

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Circuit example1

Assumption: x and $\bar{x}$ has same timing (Unrealistic assumption !)



Input variable : x

Exitation variables : Y_1 and Y_2

Secondary variables : y_1 and y_2

Outputs : Y_1 and Y_2

If not, we have two input variables x and $\bar{x}$

If we use individual gates this will be true.

Exitation functions

$$Y_1 = xy_1 + \bar{x}y_2$$

$$Y_2 = x\bar{y}_1 + \bar{x}y_2$$

Propagation delay in the combinational circuit provides a sufficient delay.

Secondary – and exitation variables ($Y_1 = y_1$ and $Y_2 = y_2$) are same in the steady-state condition, but during transition they are not.

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Circuit example1

Total states of sequential circuit consists of **stable states** and **unstable states**.

x	y_1	y_2	Y_1	Y_2
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Map for Y_1 and Y_2

2^3=8 total states

y_1y_2 \ x	0	1
00	[00]	01
01	11	[01]
11	[11]	10
10	00	[10]

Y_1Y_2

Unstable state

Stable state : $y_1y_2 = Y_1Y_2$

Transition table

Asynchronous Sequential Logic

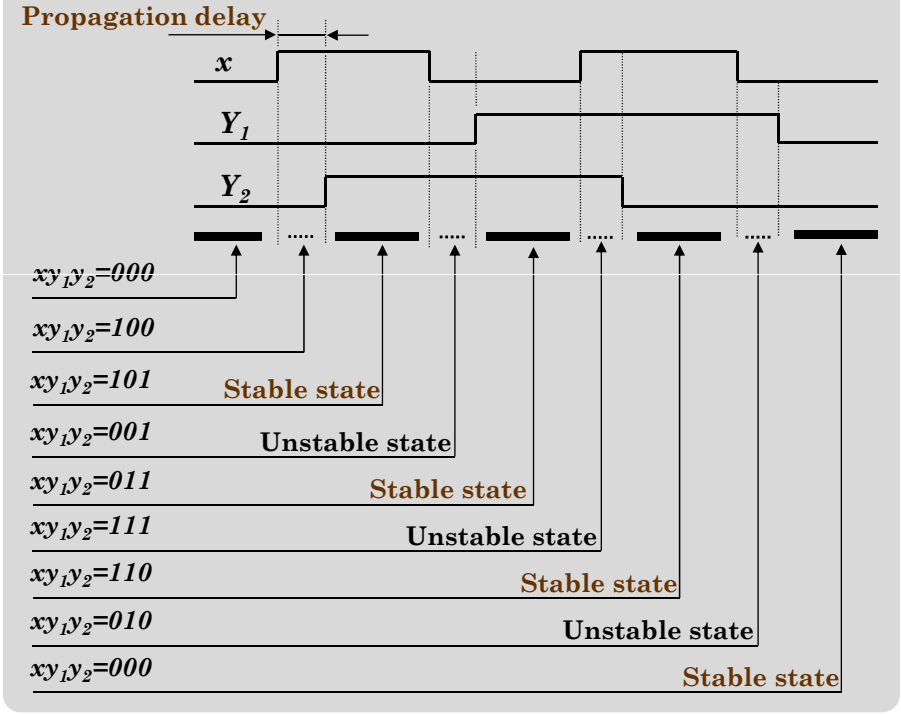
Analysis of asynchronous sequential circuits

Circuit example1

y_1y_2 \ x	0	1
00	00	01
01	11	01
11	11	10
10	00	10

Y_1Y_2

Transition table

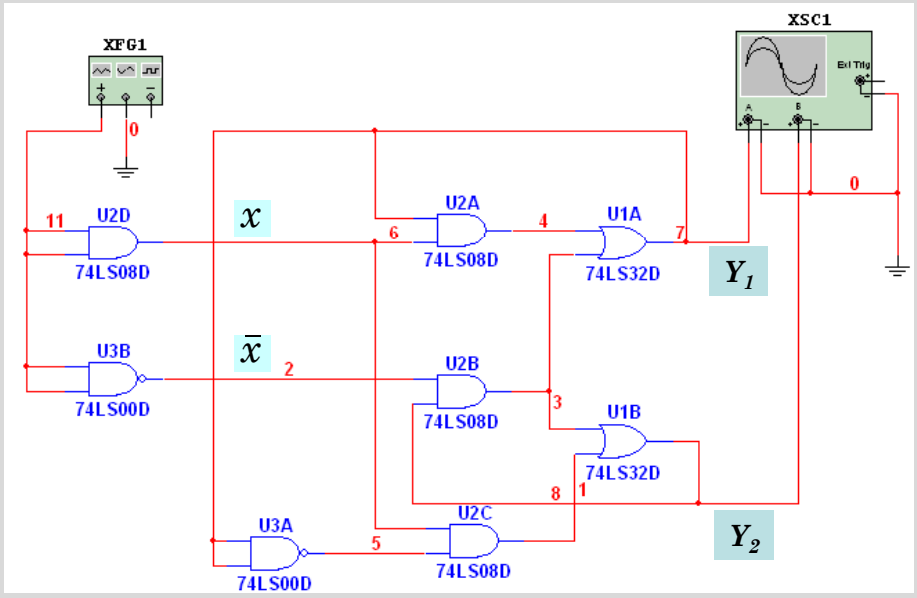


Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Simulation example1

Circuit diagram



Asynchronous Sequential Logic

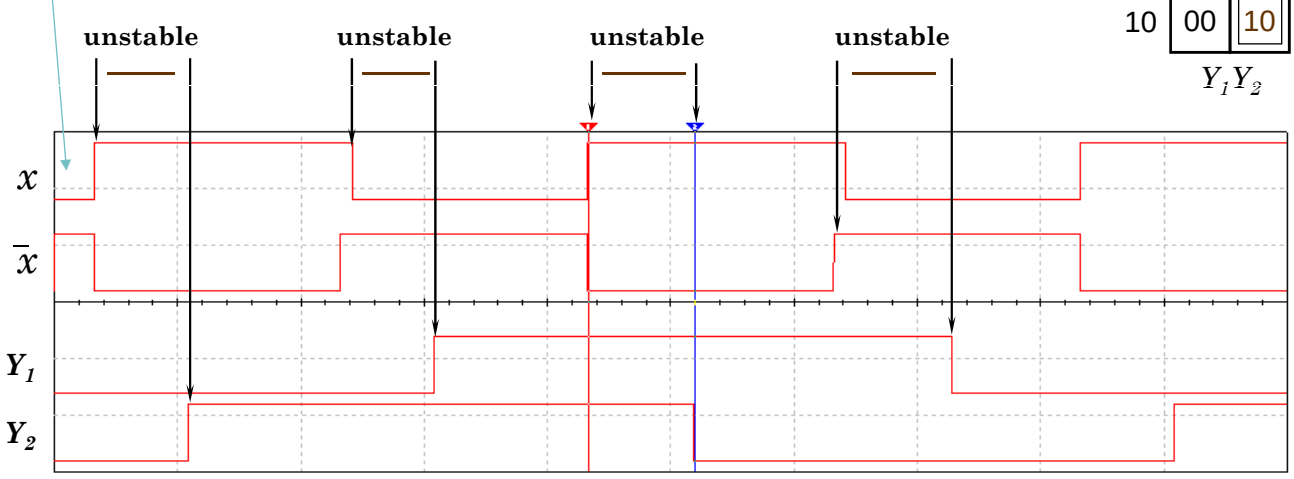
Analysis of asynchronous sequential circuits

Simulation example1

Transition table

y_1y_2 \ x	0	1
00	[00]	01
01	11	[01]
11	[11]	10
10	00	[10]

Y_1Y_2



Simulated output sequence

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Sometimes it is more convenient to name the states by letter symbols.

y_1y_2 \ x	0	1
00	[00]	01
01	11	[01]
11	[11]	10
10	00	[10]

Y_1Y_2

Transition table

a=00 , b=01 , c= 11 , d= 10

Assign binary values to the states

state \ x	0	1
a	[a]	b
b	c	[b]
c	[c]	d
d	a	[d]

Next state

Flow table

Asynchronous Sequential Logic

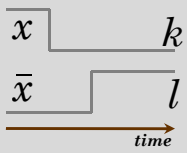
Analysis of asynchronous sequential circuits

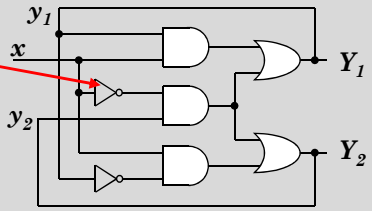
Circuit example2

Assumption: We use inverter for the complement of x

We have two input variables x and $\bar{x}$

Inverter has "large" gate delay.





$$Y_1 = ky_1 + ly_2$$
$$Y_2 = k\bar{y}_1 + ly_2$$

k l

k	l	y_1	y_2	Y_1	Y_2
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	1

Stable state

Transition table

y_1y_2 \ kl	00	01	11	10
00	00	00	01	01
01	00	11	11	01
11	00	11	11	10
10	00	00	10	10

Y_1Y_2

2^4=16 Total states

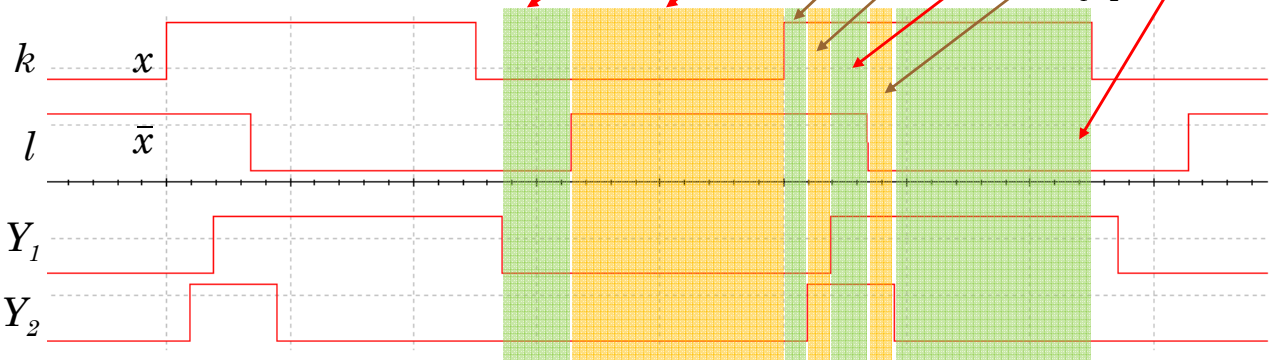
Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Simulation result of example2

y_1y_2 \ kl	00	01	11	10
00	00	00	01	01
01	00	11	11	01
11	00	11	11	10
10	00	00	10	10

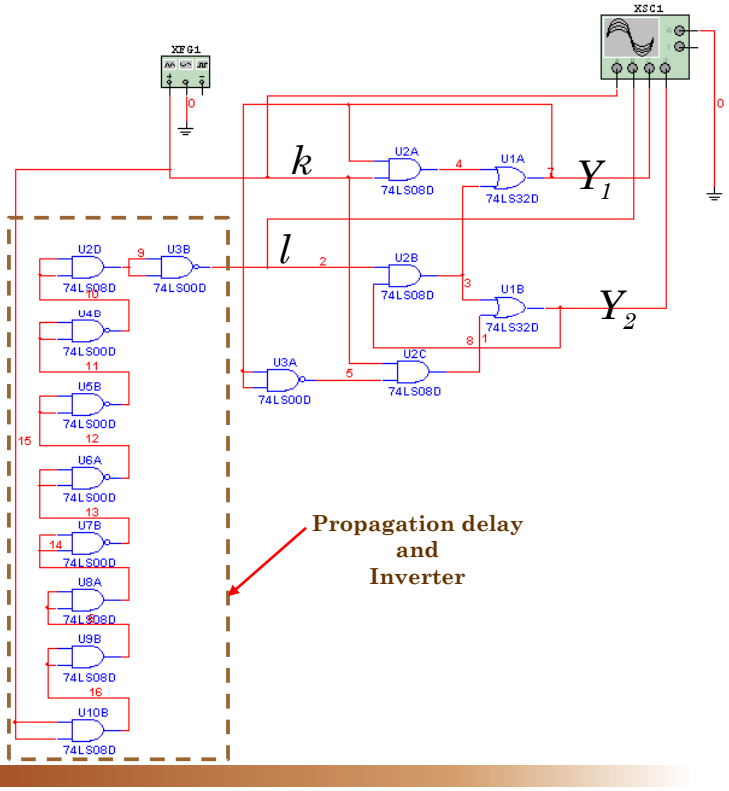
Y_1Y_2



Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

Circuit diagram for simulation of example2

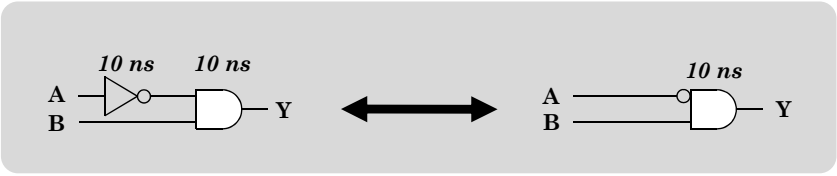


Asynchronous Sequential Logic

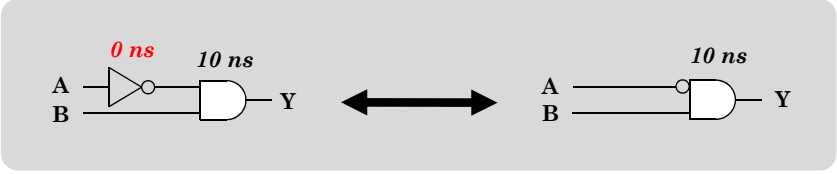
Analysis of asynchronous sequential circuits

Convention for gate delays in circuit diagrams

Only LOGICAL equality



LOGICAL equality *Equal TIMING*



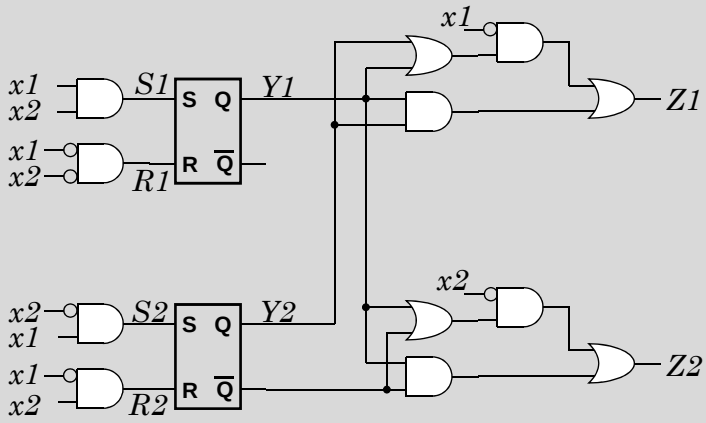
Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits — **SR latch in asynchronous sequential circuit**

Example

$$S_1 = x_1 x_2 \quad R_1 = \bar{x}_1 \bar{x}_2$$
$$S_2 = x_1 \bar{x}_2 \quad R_2 = \bar{x}_1 x_2$$
$$Z_1 = \bar{x}_1 (y_1 + y_2) + y_1 y_2$$
$$Z_2 = \bar{x}_2 (y_1 + \bar{y}_2) + y_1 \bar{y}_2$$

Boolean functions



Example Circuit

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits — **SR latch in asynchronous sequential circuit**

x_1x_2	y_1y_2	z_1z_2
00	00	01
00	01	10
00	11	11
00	10	11
01	00	00
01	01	10
01	11	10
01	10	11
11	00	00
11	01	00
11	11	10
11	10	01
10	00	01
10	01	00
10	11	11
10	10	01

Total state table

x_1x_2	y_1y_2	Y_1Y_2	z_1z_2
00	00	00	01
00	01	01	10
00	11	01	11
00	10	00	11
01	00	00	00
01	01	00	10
01	11	10	10
01	10	10	11
11	00	10	00
11	01	11	00
11	11	11	10
11	10	10	01
10	00	01	01
10	01	01	00
10	11	11	11
10	10	11	01

Transition table

How we find columns Y_1 and Y_2?

y_1y_2 \ x_1x_2	00	01	11	10
00	00	00	10	01
01	01	00	11	01
11	01	10	11	11
10	00	10	10	11

Y_1Y_2

Transition table

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

SR latch in asynchronous sequential circuit

x_1x_2	y_1y_2	S_1R_1	S_2R_2	Y_1Y_2
0 0	0 0	0 1	0 0	0 0
0 0	0 1	0 1	0 0	0 1
0 0	1 1	0 1	0 0	0 1
0 0	1 0	0 1	0 0	0 0
0 1	0 0	0 0	0 1	0 0
0 1	0 1	0 0	0 1	0 0
0 1	1 1	0 0	0 1	1 0
0 1	1 0	0 0	0 1	1 0
1 1	0 0	1 0	0 0	1 0
1 1	0 1	1 0	0 0	1 1
1 1	1 1	1 0	0 0	1 1
1 1	1 0	1 0	0 0	1 0
1 0	0 0	0 0	1 0	0 1
1 0	0 1	0 0	1 0	0 1
1 0	1 1	0 0	1 0	1 1
1 0	1 0	0 0	1 0	1 1

Latch exitation table with exitation variables

$$S_1 = x_1x_2 \quad R_1 = \bar{x}_1\bar{x}_2 \quad S_2 = x_1\bar{x}_2 \quad R_2 = \bar{x}_1x_2$$

y_1y_2 \ x_1x_2	00	01	11	10
00	01,00	00,01	10,00	00,10
01	01,00	00,01	10,00	00,10
11	01,00	00,01	10,00	00,10
10	01,00	00,01	10,00	00,10

S_1R_1, S_2R_2

Latch exitation table

Present state y_1y_2

Next state Y_1Y_2

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

SR latch in asynchronous sequential circuit

$y \rightarrow Y$		$S\ R$
0	0	0 X
0	1	1 0
1	0	0 1
1	1	X 0

$x \equiv 0$ *or* 1

Note!

SR=11 input state is forbidden

For example: transition from state 0 to state 0

SR=01 force to state 0

SR=00 use original state 0

transition from state 1 to state 0

SR=01 force to state 1

transition from state 1 to state 1

SR=10 force to state 1

SR=00 use original state 1

Use latch exitation table to find states of exitation variables Y

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

y_1y_2 \ x_1x_2	00	01	11	10
00	01	00	00	01
01	10	10	00	00
11	11	10	10	11
10	11	11	01	01

z_1z_2

Output table

s \ x_1x_2	00	01	11	10
a	a	a	d	b
b	b	a	c	b
c	b	d	c	c
d	a	d	d	c

S

Flow table

$a = y_1y_2 = 00$
$b = 01$
$c = 11$
$d = 10$

$$Z_1 = \bar{x}_1(y_1 + y_2) + y_1y_2$$
$$Z_2 = \bar{x}_2(y_1 + \bar{y}_2) + y_1\bar{y}_2$$

→ Output table, Flow table → Time sequence of outputs

Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits

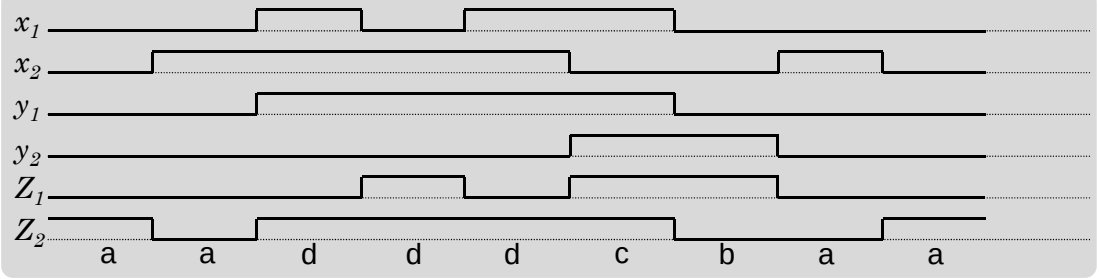
y_1y_2 \ x_1x_2	00	01	11	10
00	01	00	00	01
01	10	10	00	00
11	11	10	10	11
10	11	11	01	01

Z_1Z_2

Flow tables

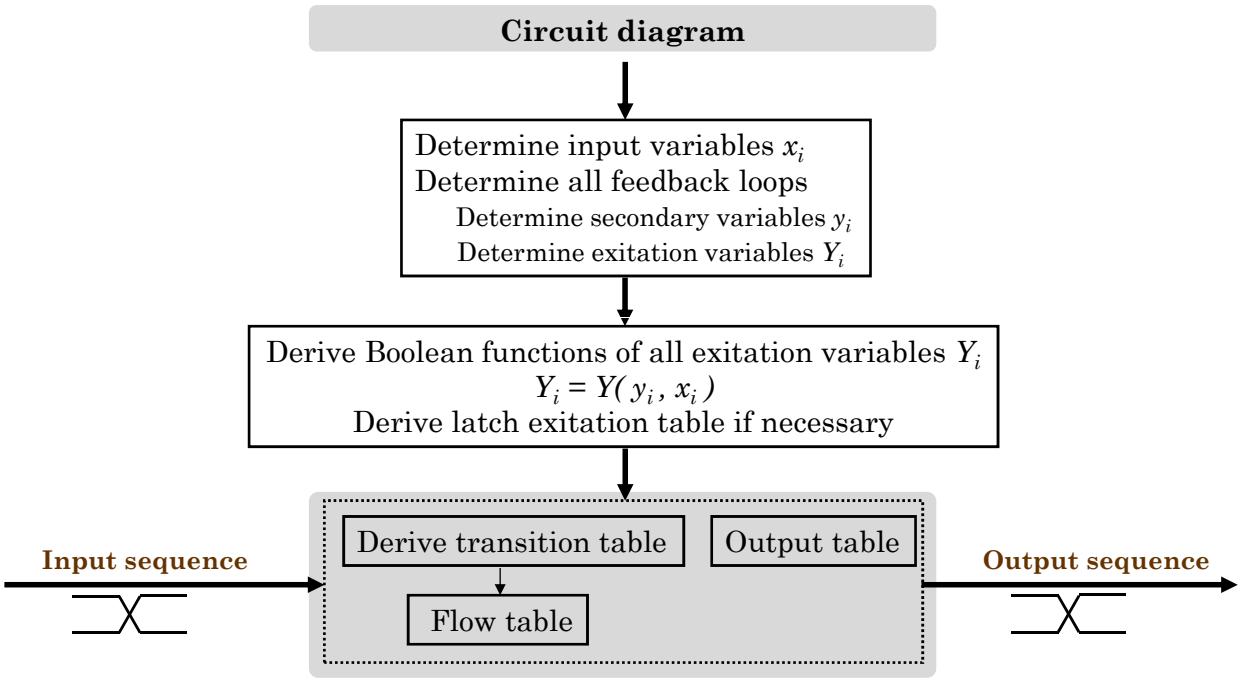
s \ x_1x_2	00	01	11	10
a	a	a	d	b
b	b	a	c	b
c	b	d	c	c
d	a	d	d	c

S



Asynchronous Sequential Logic

Analysis of asynchronous sequential circuits



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