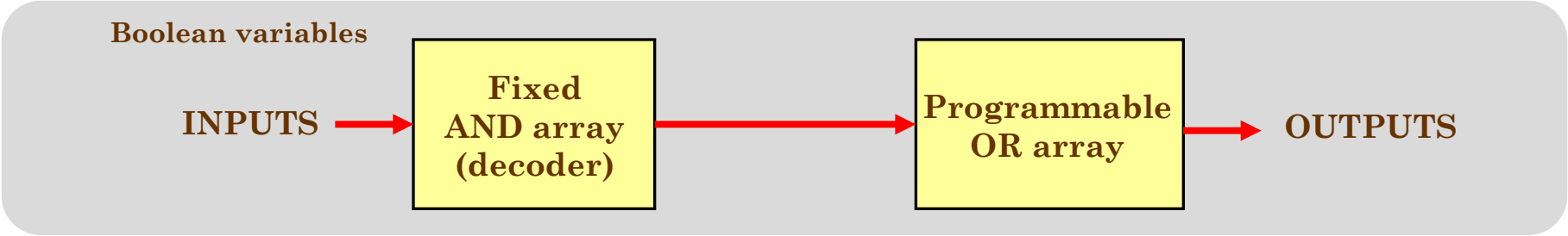
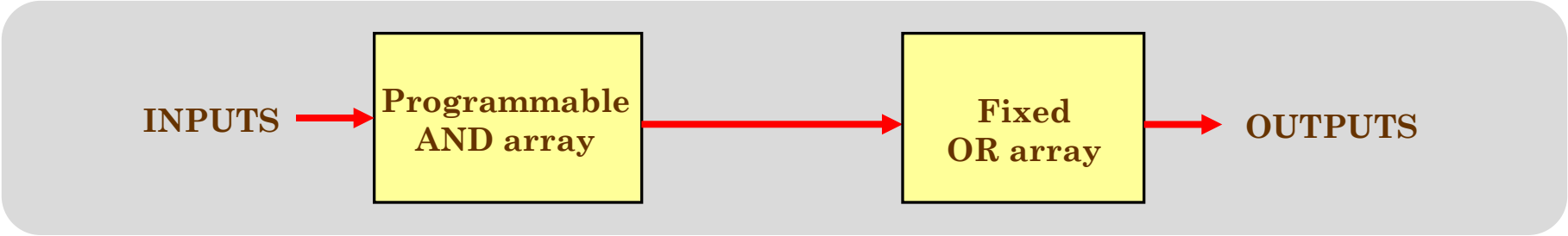
Combinational PLDs (Programmable Logic Devices)

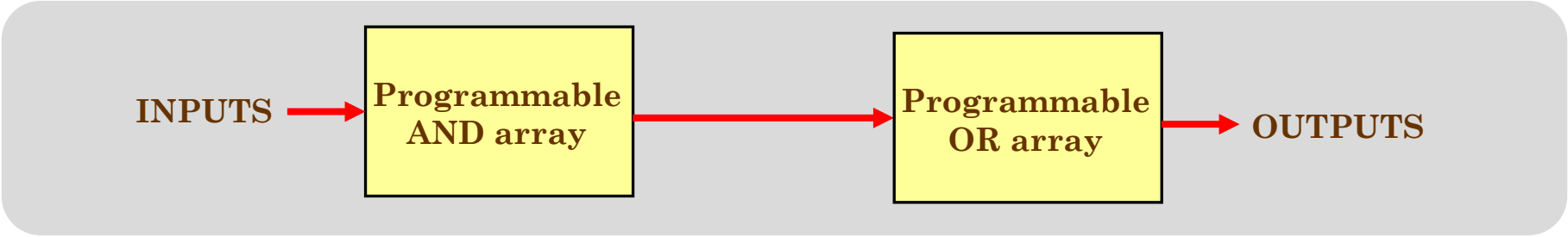
Basic Configuration of three PLDs



Programmable Read-Only Memory (PROM)



Programmable Array Logic (PAL)

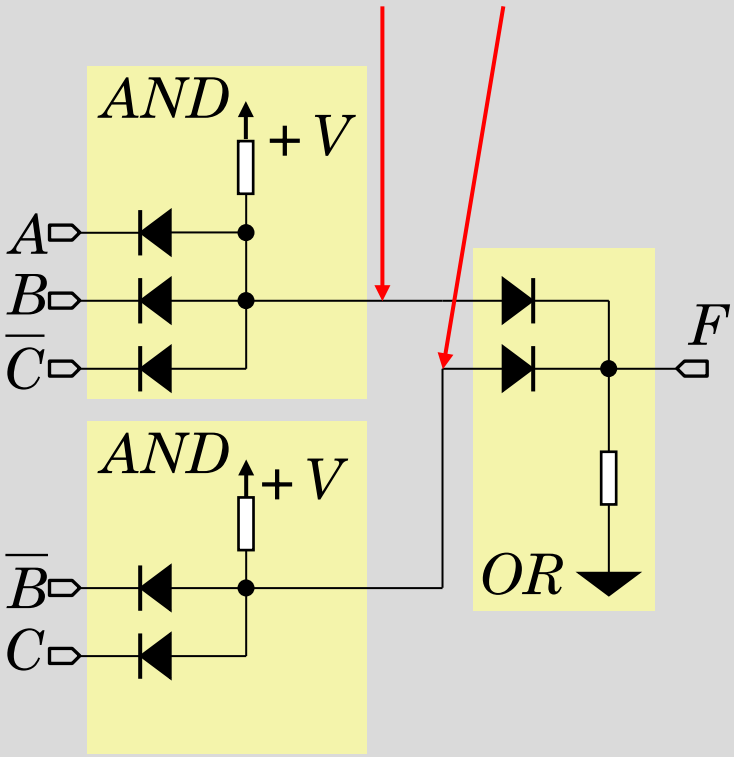


(Field) Programmable Logic Array (PLA)

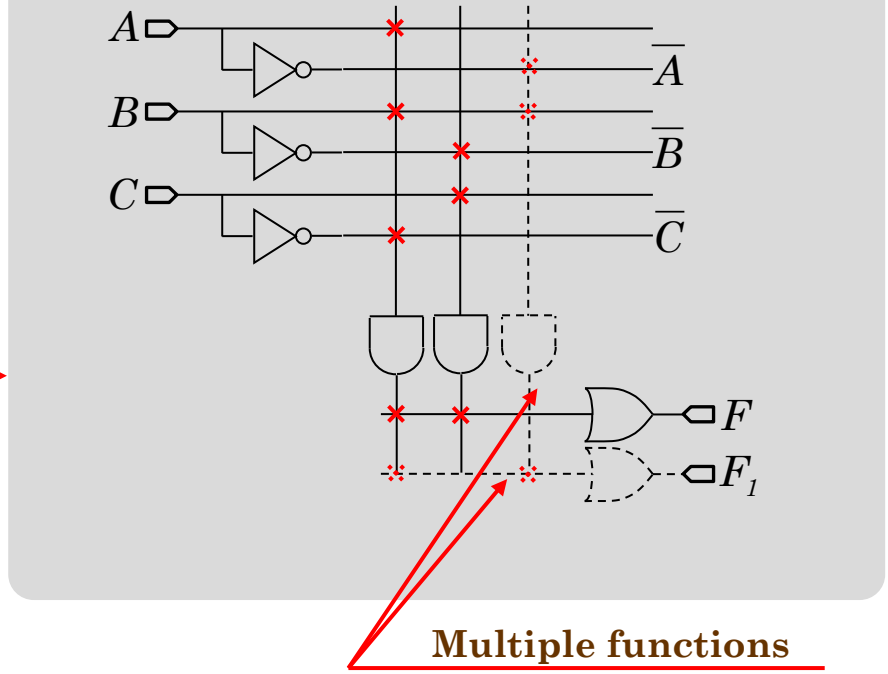
Combinational PLDs (Programmable Logic Devices)

Two-level AND-OR Arrays

$$F(C,B,A) = \overline{C}BA + C\overline{B}$$



Simplified equivalent circuit for two-level AND-OR array

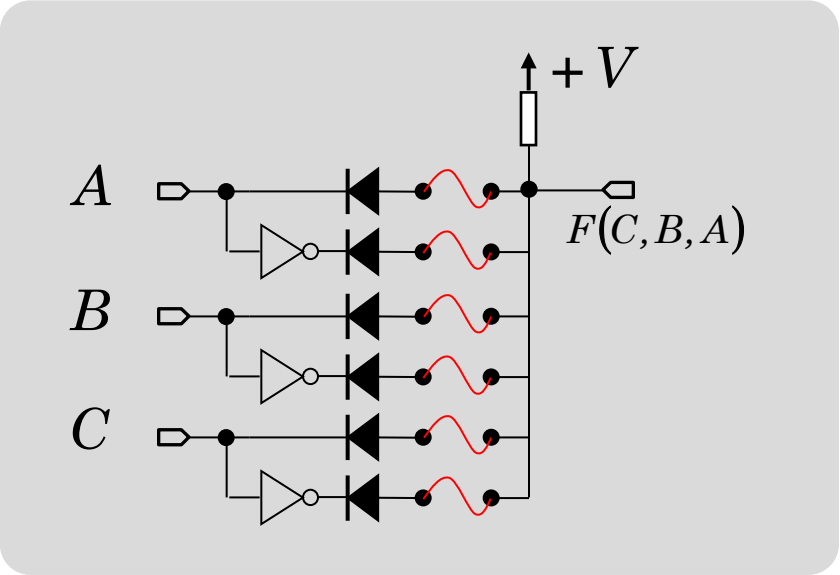


Multiple functions

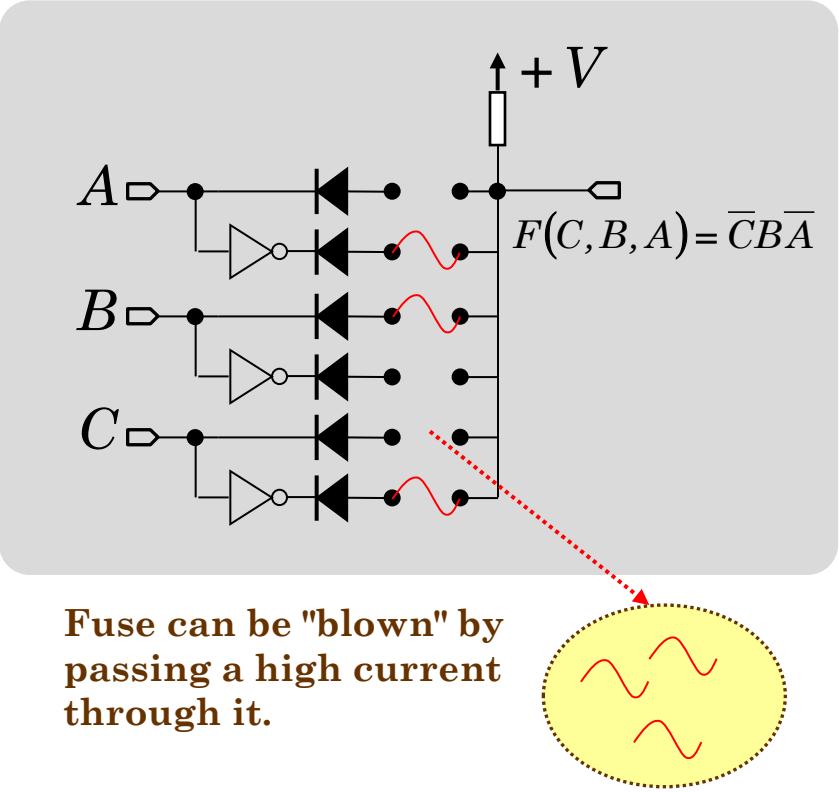
Combinational PLDs (Programmable Logic Devices)

Field-programmable AND and OR Arrays

Field-programmable logic elements are devices that contain uncommitted AND/OR arrays that are (programmed) configured by the designer.



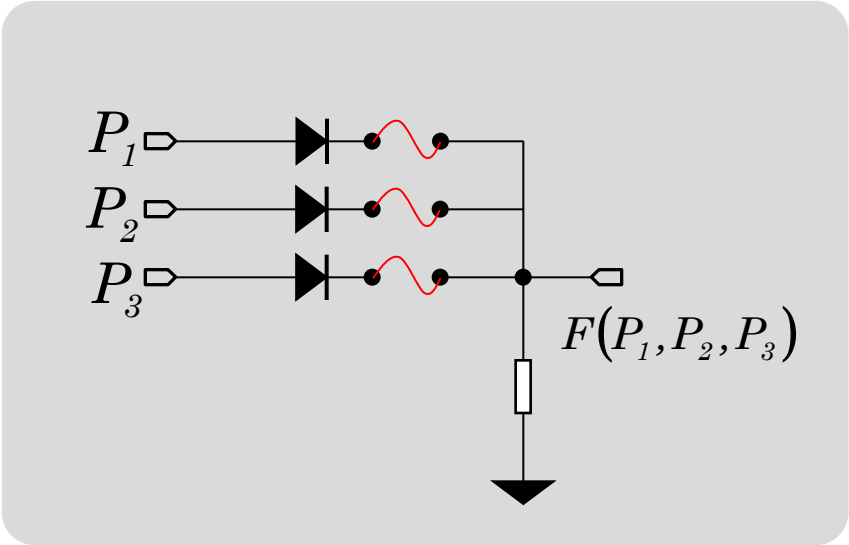
Unprogrammed AND array



Fuse can be "blown" by passing a high current through it.

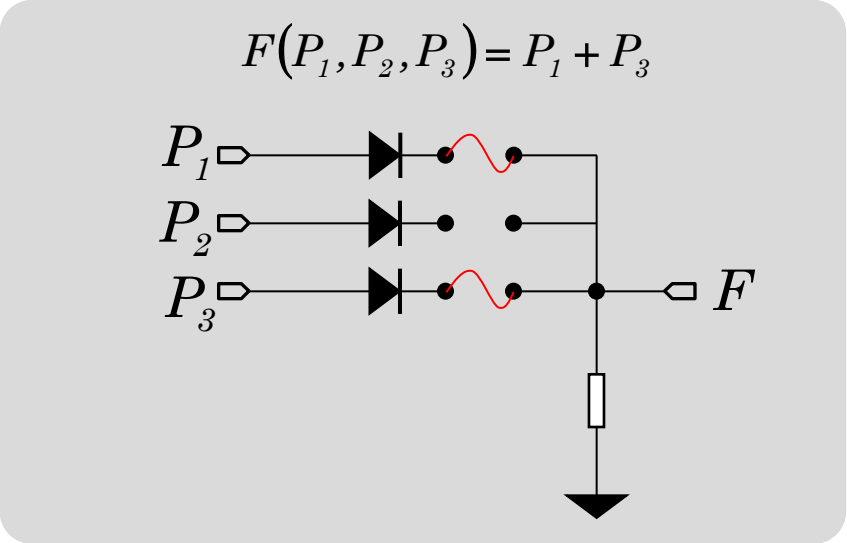
Combinational PLDs (Programmable Logic Devices)

Field-programmable AND and OR Arrays

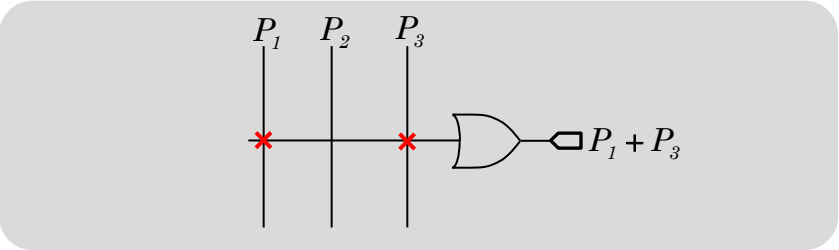


Unprogrammed OR array

$$F(P_1, P_2, P_3) = P_1 + P_3$$

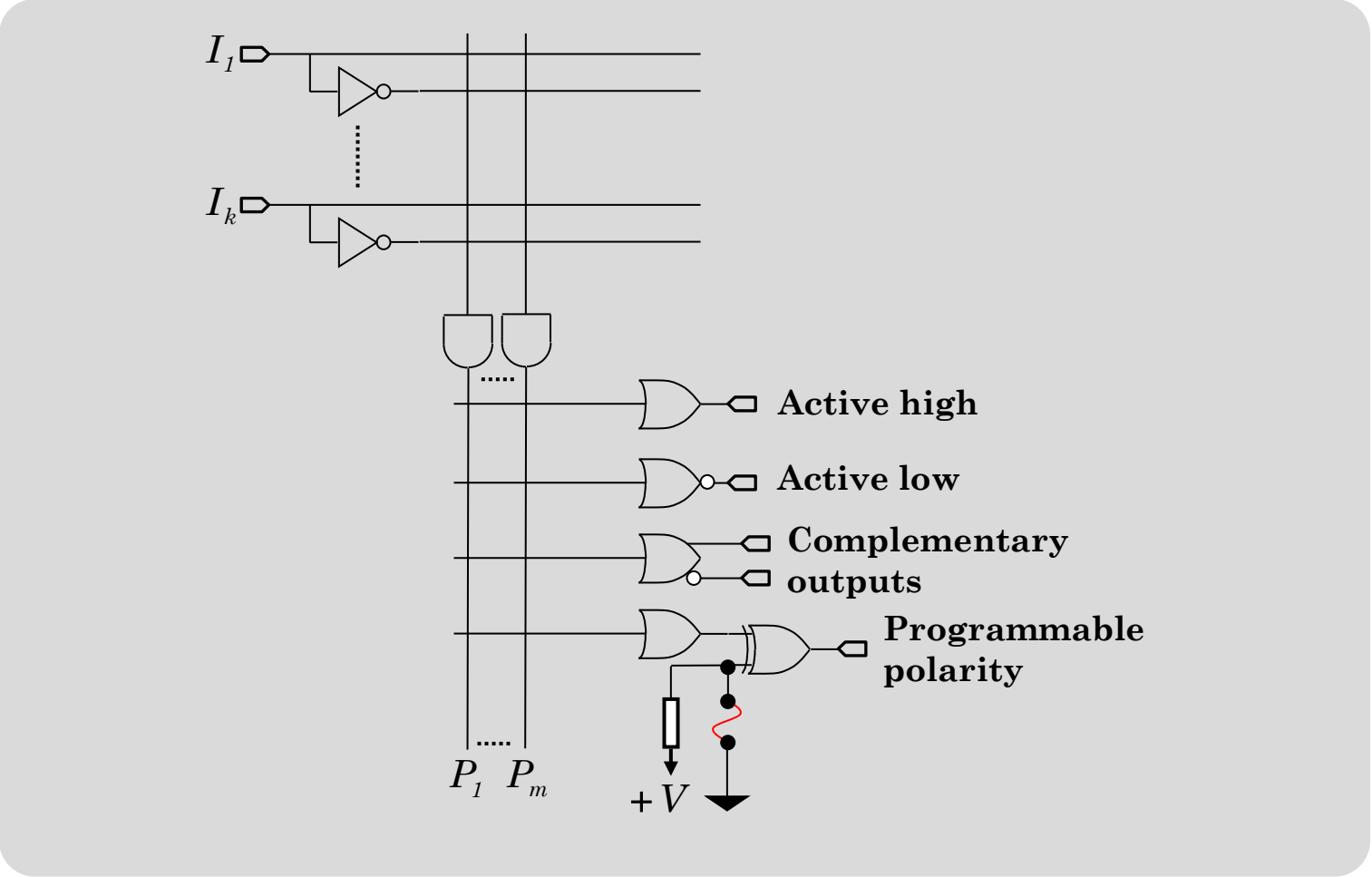


Programmed OR array



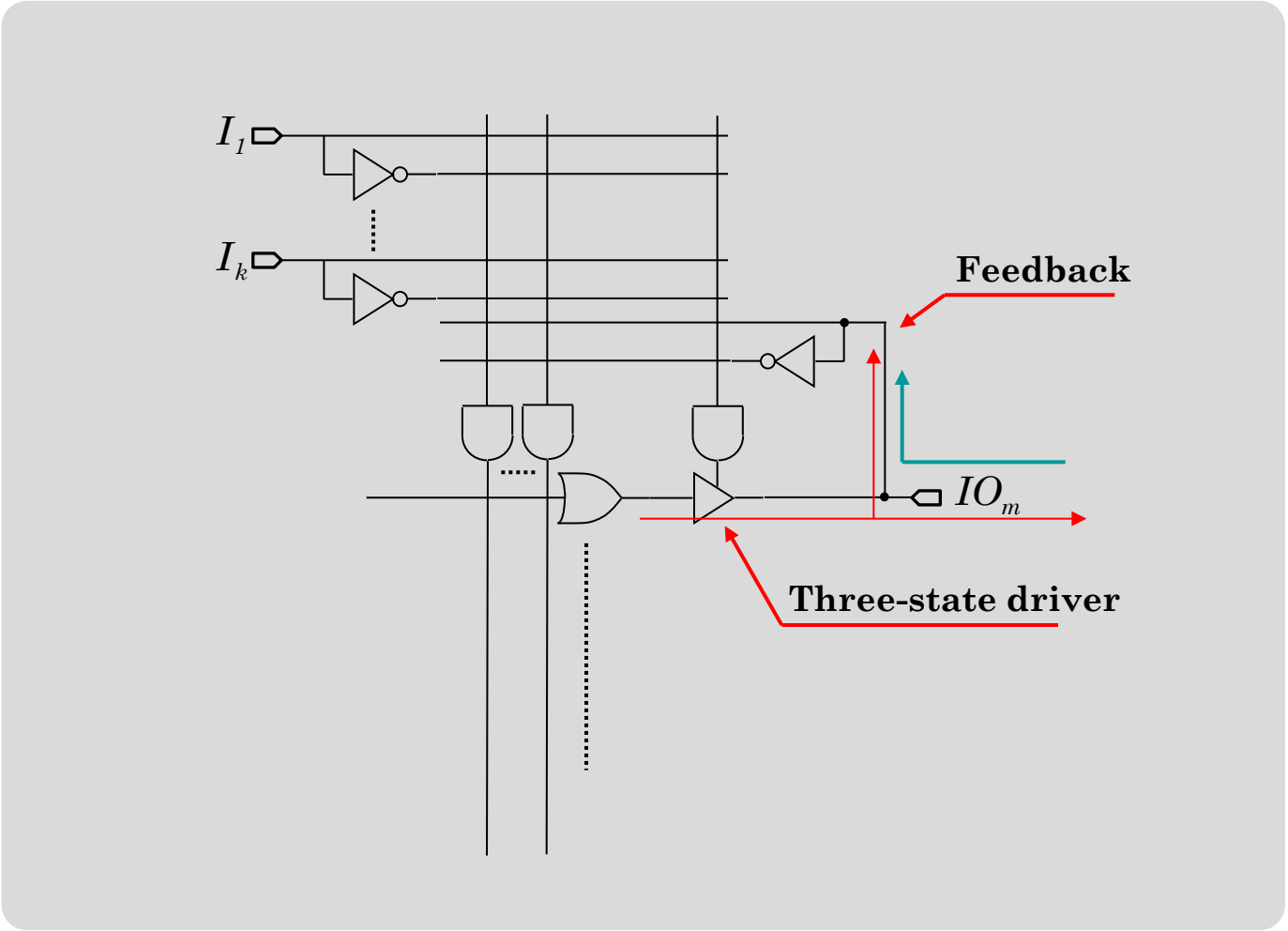
Combinational PLDs (Programmable Logic Devices)

Output Polarity Options



Combinational PLDs (Programmable Logic Devices)

Bidirectional Pins and Feed back Lines



Combinational PLDs (Programmable Logic Devices)

PLA (Programmable Logic Array)

If we use ROM to implement the Boolean function we will waste the silicon area.

All Input combinations are implemented in ROM (address decoder).

Usually we must implement only few minterms.

$\Rightarrow$ **Only few OR-operators.**

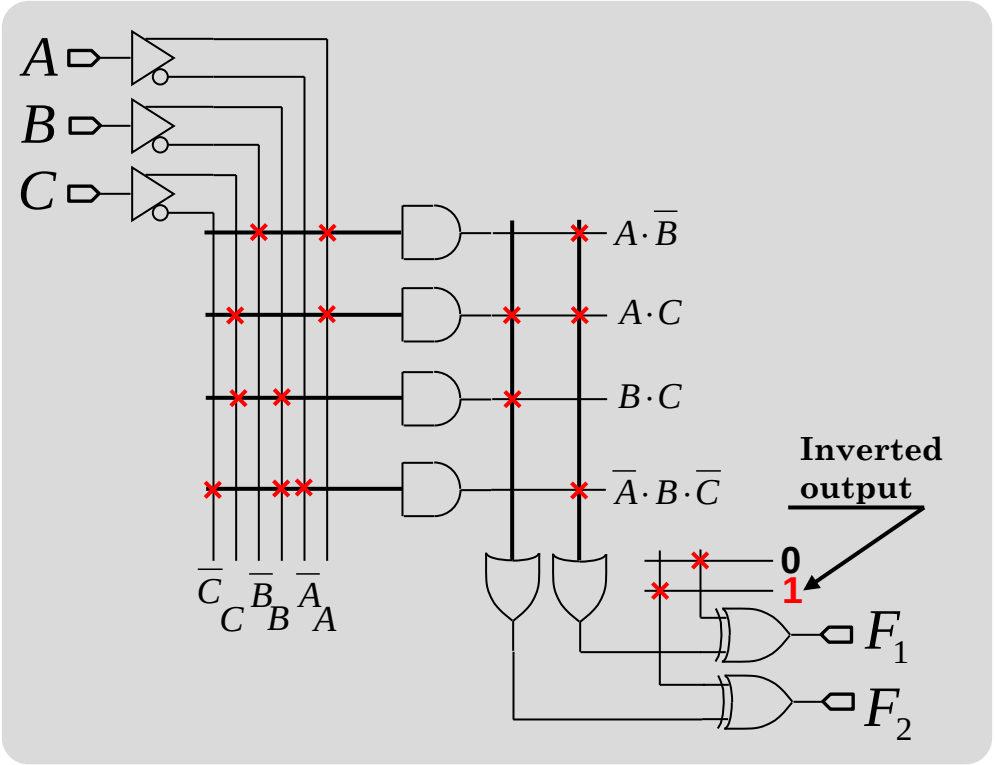
$\Rightarrow$

The standard SOP format has few OR operations and several input variables.

PLA saves silicon area

$$F_1 = \overline{B} \cdot A + C \cdot A + \overline{C} \cdot B \cdot \overline{A}$$

$$F_2 = \overline{C \cdot A + B \cdot C}$$

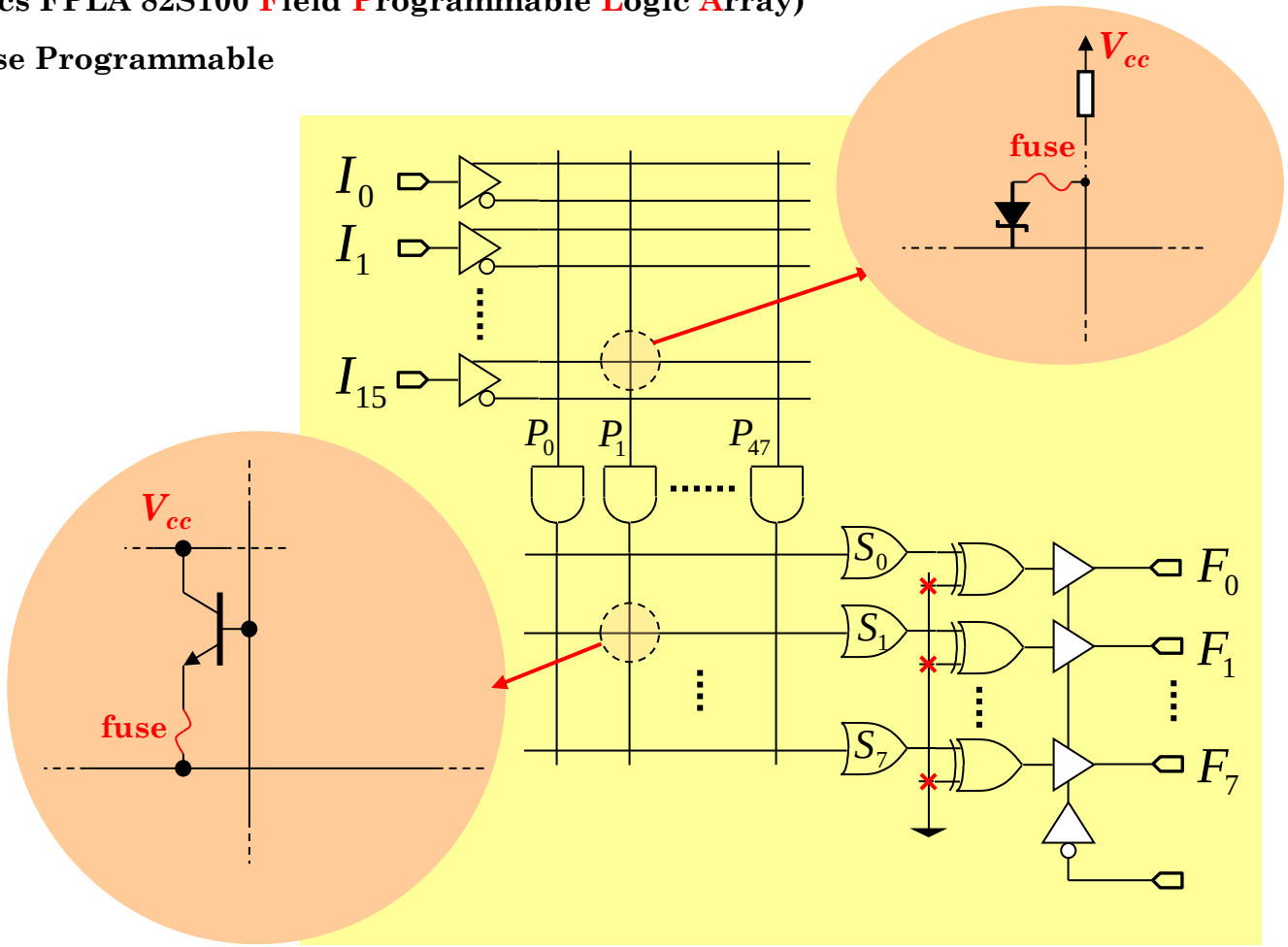


Combinational PLDs (Programmable Logic Devices)

PLA (Programmable Logic Array)

Example (Old Signetics FPLA 82S100 Field Programmable Logic Array)

82S100 is 16X48X8 Fuse Programmable Logic Array circuit

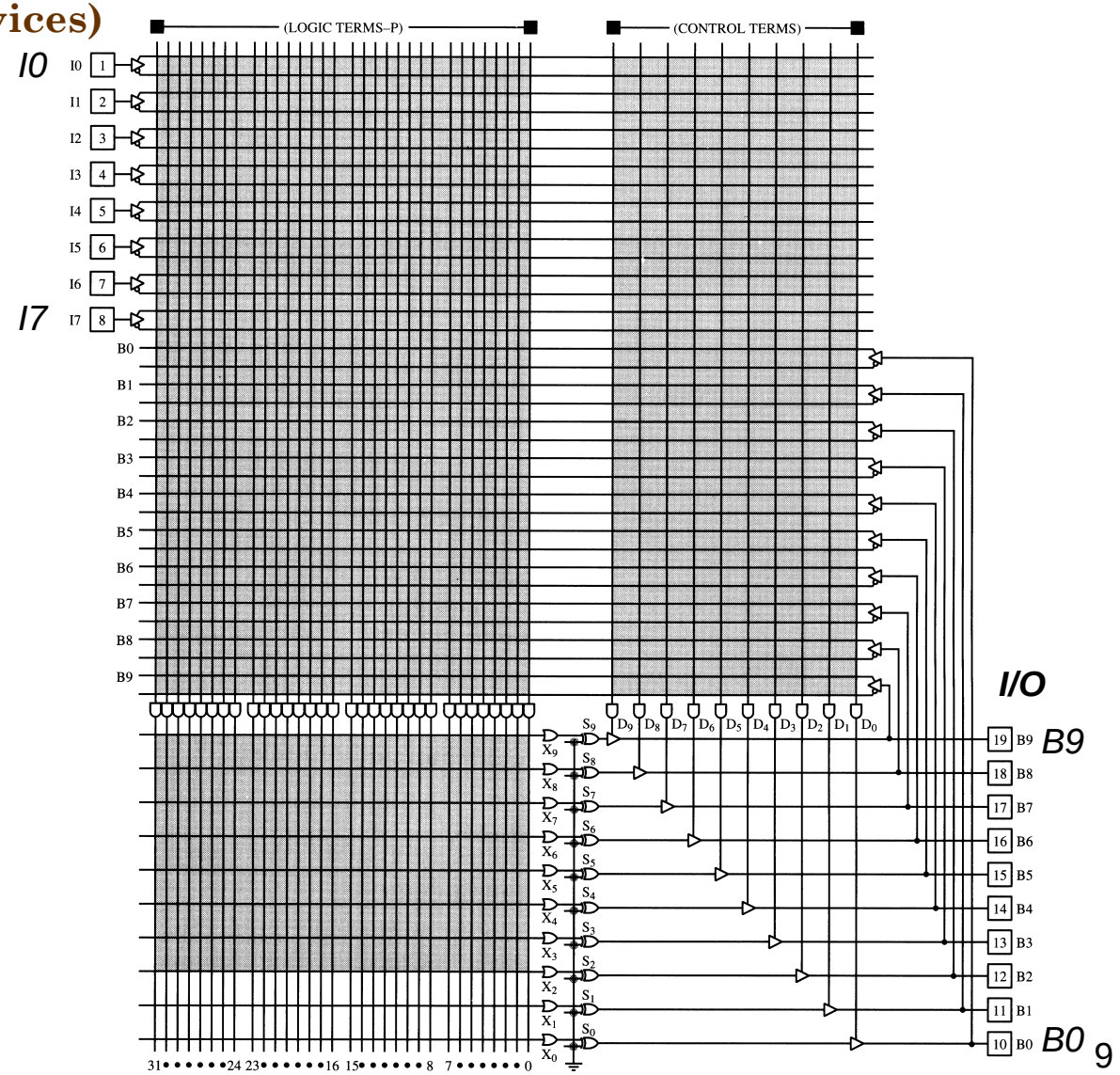


Combinational PLDs (Programmable Logic Devices)

PLA (Programmable Logic Array)

Example of FPLA Device

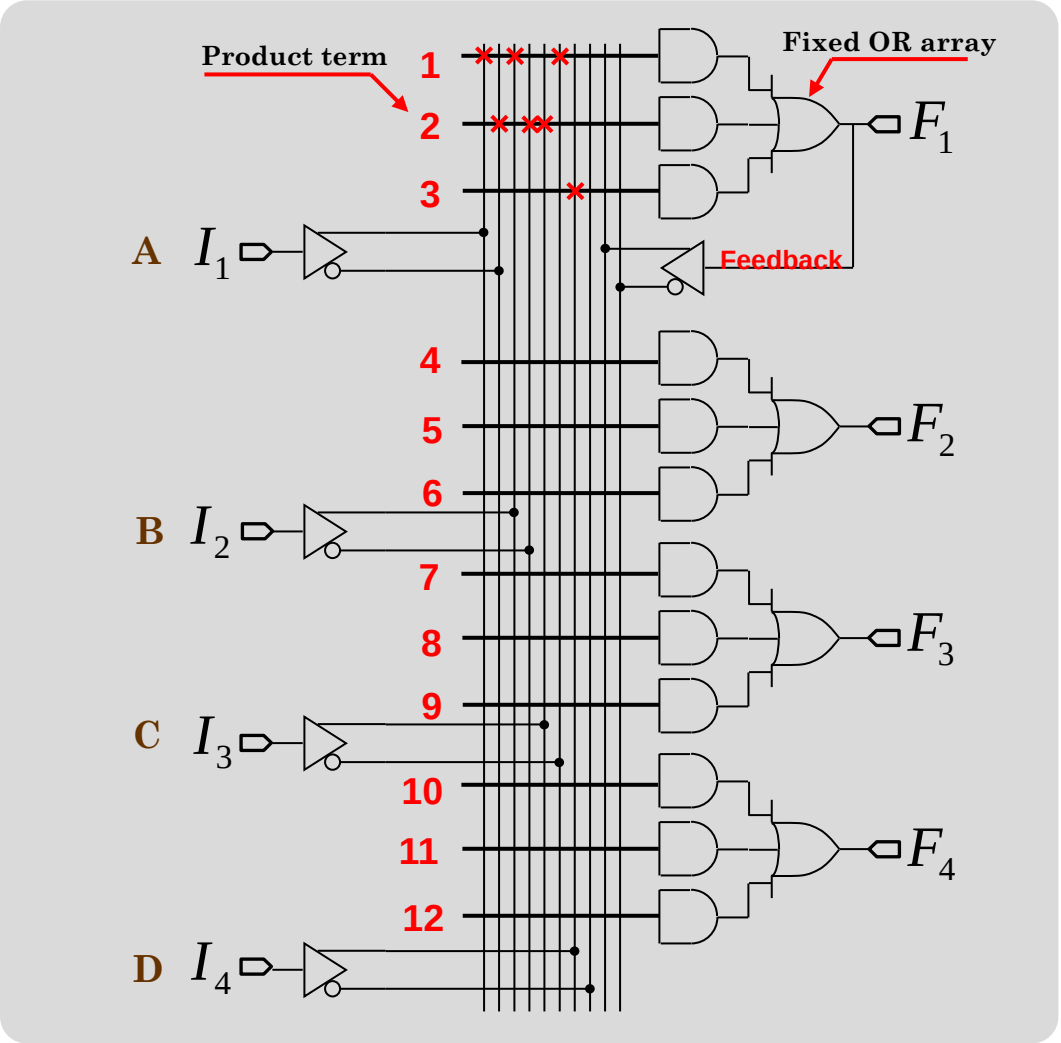
Philips PLS153A



Combinational PLDs (Programmable Logic Devices)

PAL (Programmable Array Logic)

$$F_1 = A \cdot B \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + D$$

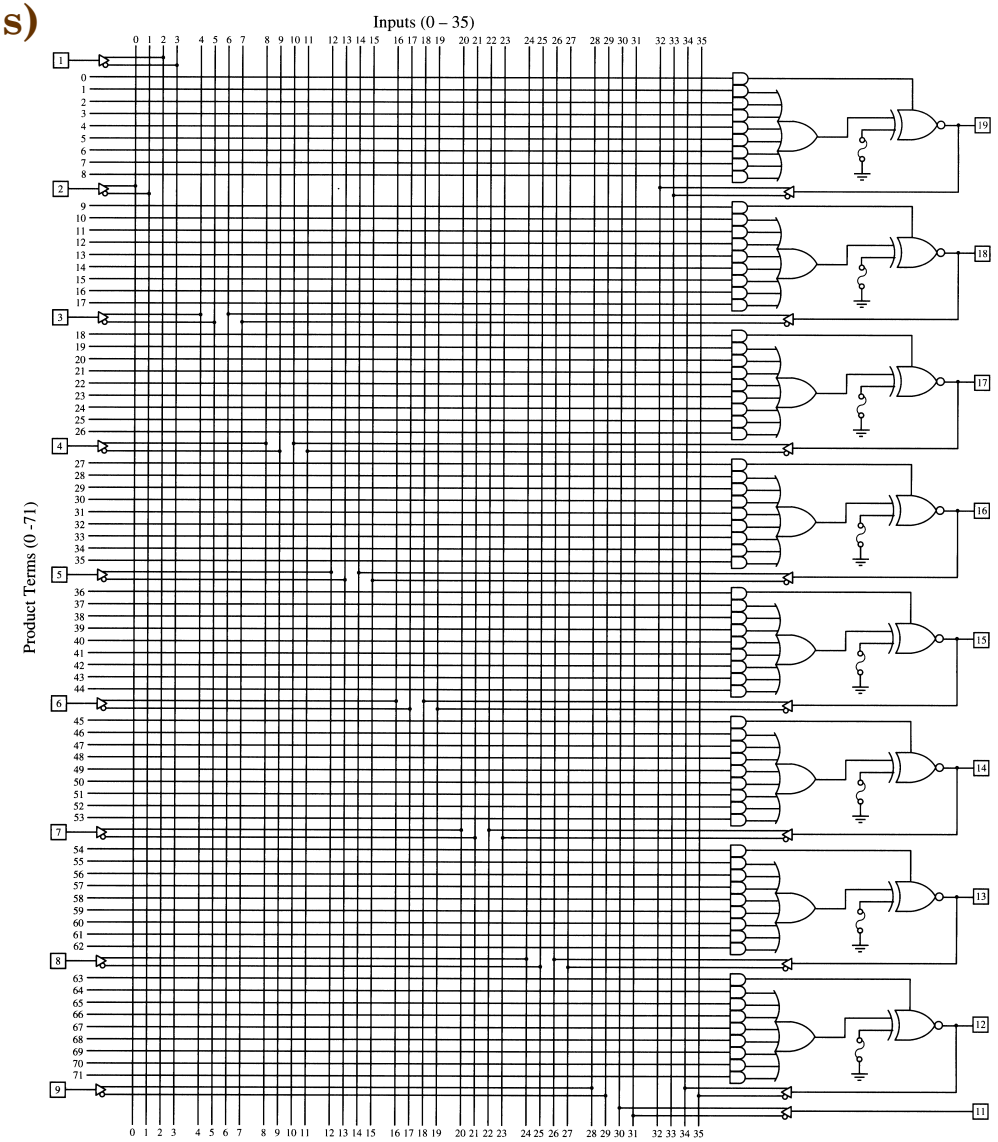


Combinational PLDs (Programmable Logic Devices)

PAL (Programmable Array Logic)

Example of PAL Device

AMD PAL18P8

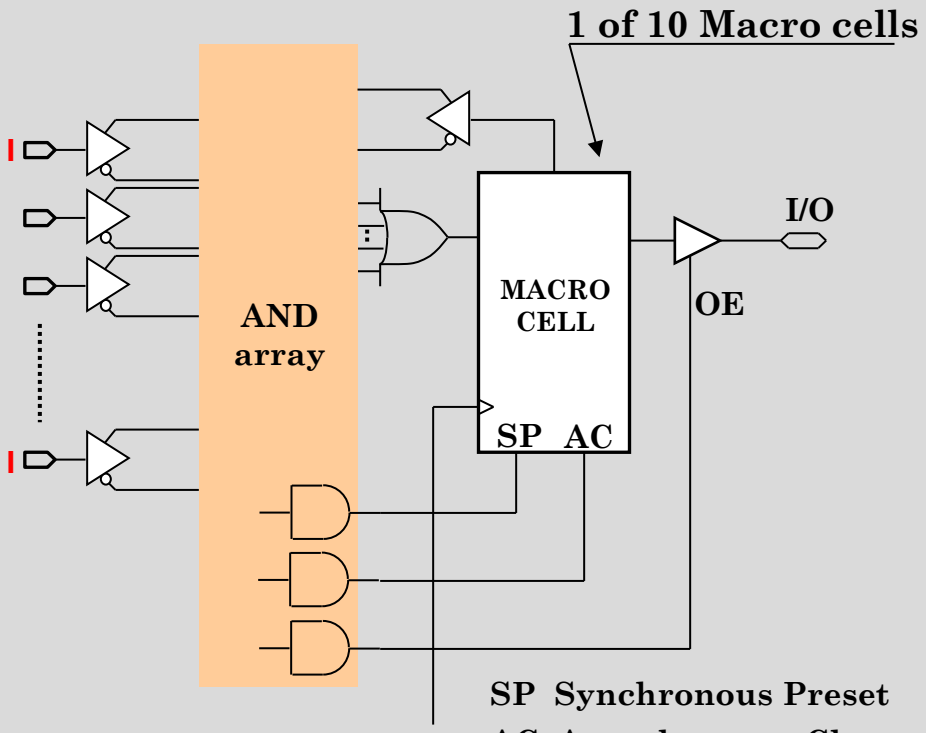


Combinational PLDs (Programmable Logic Devices)

PAL (Programmable Array Logic)

Combinational logic + D-flip-flops ← (for sequential circuit applications)

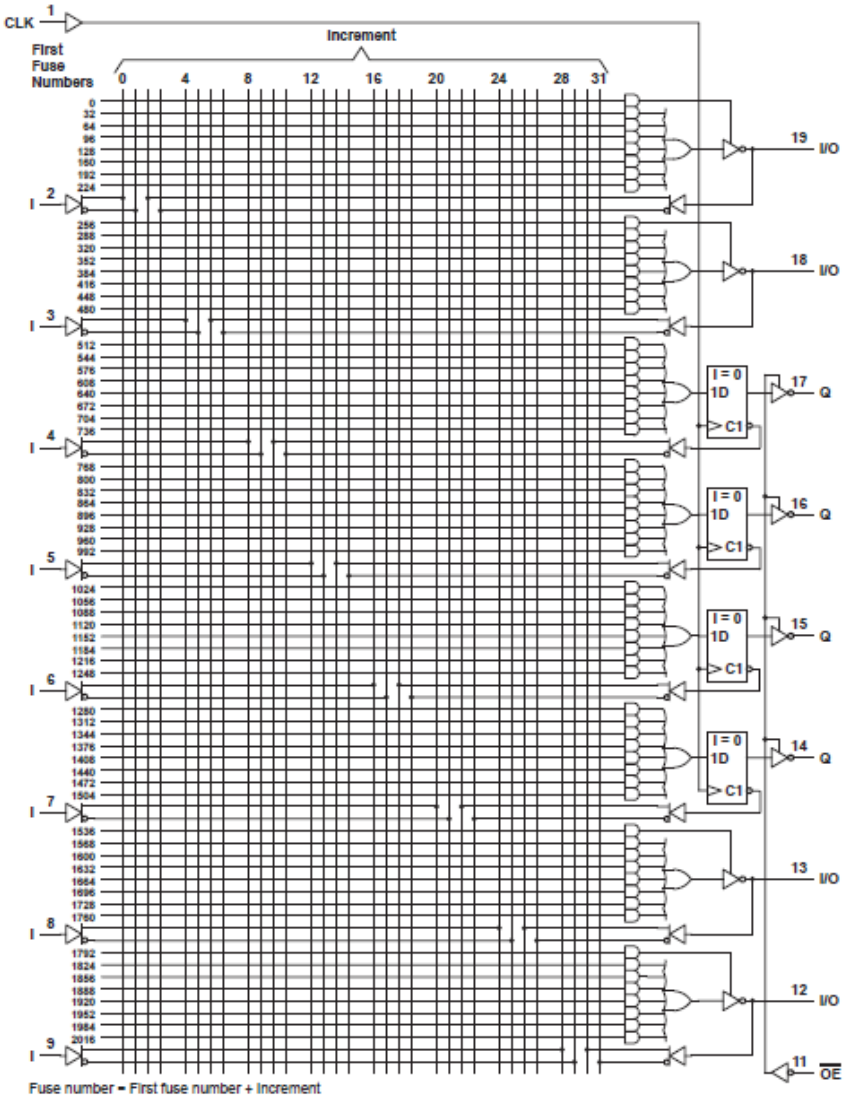
One example : PEEL 22CV10A Electrically Erasable



SP Synchronous Preset
AC Asynchronous Clear
OE Output Enable

Combinational PLDs (Programmable Logic Devices)

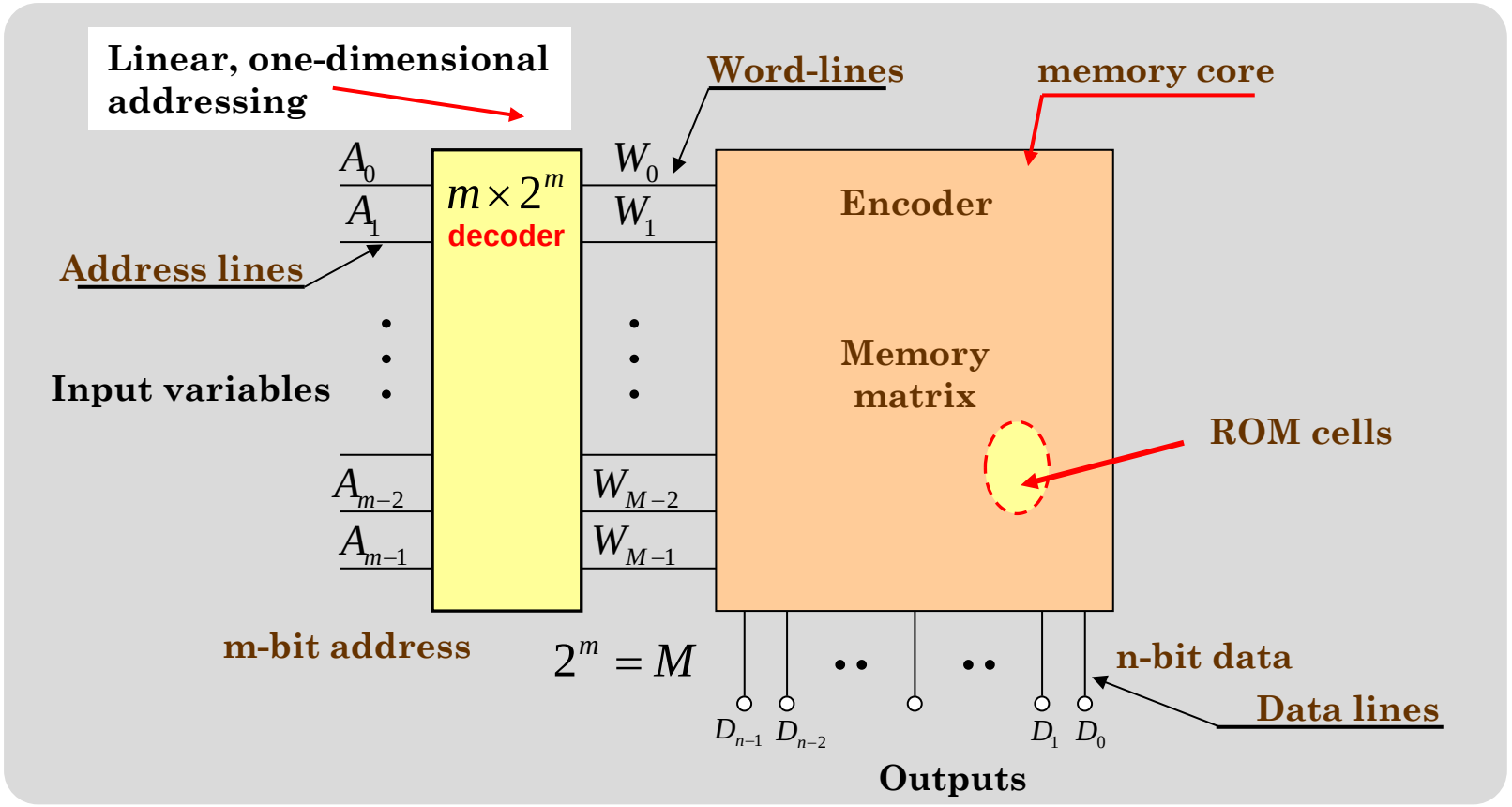
PAL16R4AM



Combinational PLDs (Programmable Logic Devices)

ROM implementation

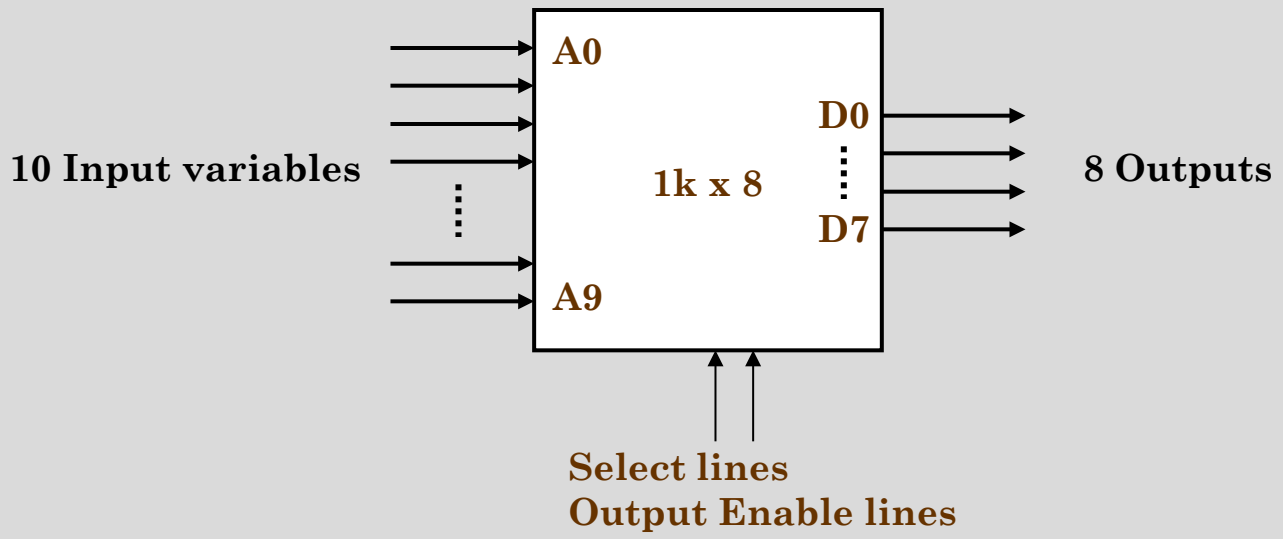
m inputs (address $A_i = 2^m$ combinations) → $2^m \times n$ ROM → *n outputs (data)*



Combinational PLDs (Programmable Logic Devices)

ROM implementation

Canonical SOP form of the Boolean function : Minterms ⟷ Address locations



Combinational PLDs (Programmable Logic Devices)

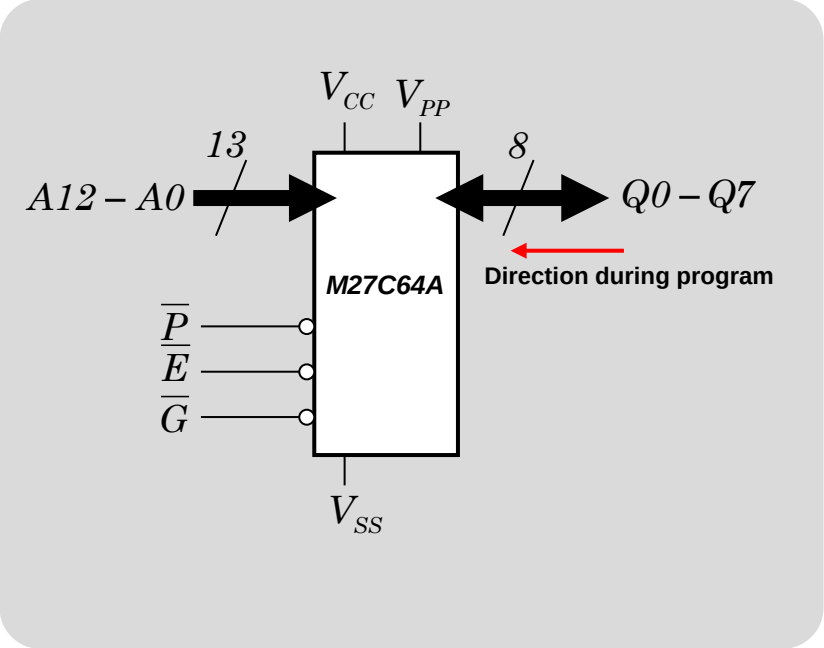
ROM implementation

Example

13 input variables *In12 - In0*
8 different switching functions *F7-F0*

ROM organized as 8Kb x 8 (8192x8bits)

For example M27C64A UV EPROM



Logic diagram

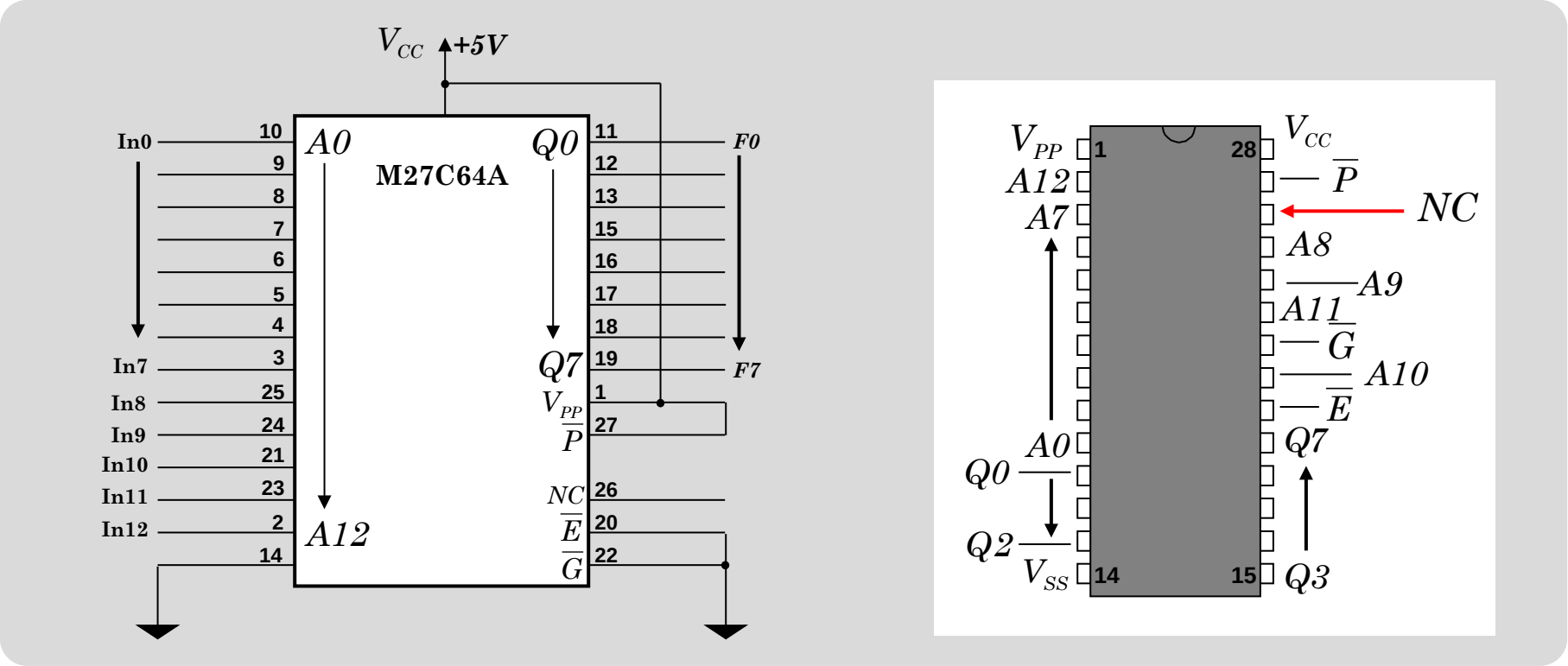
V_{CC}	Supply voltage +5V (10%)
V_{SS}	Ground
V_{PP}	Program Supply 12.5V +- 0.25V
$\overline{P}$	Program
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$A12 - A0$	Address Inputs
$Q7 - Q0$	Data Outputs

Signal Names

Combinational PLDs (Programmable Logic Devices)

ROM implementation

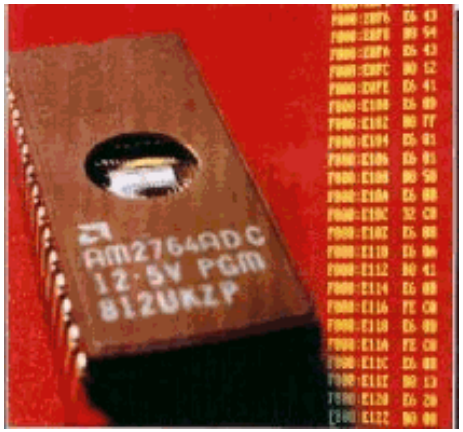
Example



Implemented combinational logic

Dip Connections

ROM implementation



Universal Programmer

UV Eraser

Combinational PLDs (Programmable Logic Devices)

Programming Software

Examples (free download)

ATMEL : WinCUPL software

SPLDs Simple Programmable Logic Devices (16V8, 20V8, 22V10)

ATF22LV10ZQZ

CPLDs Complex Programmable Logic Devices

ATF15xxBE family
ATV750B

XILINX : Xilinx ISE Design Suite (Schematics, VHDL, Verilog)

CPLDs Complex Programmable Logic Devices

XC95xx family

FPGAs Field Programmable Gate Arrays

Virtex, Spartan,..

The End