# Semiconductor Memories

## Introduction

### Classification of Memory Devices

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"Combinational Logic"
Linear Addressing

- **m inputs (address $A_i = 2^m$ combinations)**
- **$2^m \times n$ ROM**
- **n outputs (data)**

Linear, one-dimensional addressing

- Address lines
  - $n < m$
  - $n > m$
  - $n = m$

- m-bit address
- $2^m = M$

To Sense Amplifiers

- Encoder
- Memory matrix
- Word-lines
- Memory core
- ROM Cell
- n-bit data
- Data lines

- $\text{ROM (Read Only Memory)}$
The Cell is designed so that a 0 or 1 is presented to the bit line $D_i$ upon activation of its word line $W_j$.

- Diode-based ROM Cell
- MOSFET-based ROM Cell
- BJT-based ROM Cell
Disadvantage of the diode cell:

No isolation between the word line $W_j$ and the bit line $D_i$. The $W_j$ driver must provide quite high current to charge capacitance $C_{tot}$. (And discharge $C_{Wj}$)

This approach works only for small memories.

$$C_{tot(max)} \approx C_{Wj} + \sum_{i=1}^{n} C_{Di}$$

$n = \text{number of data bits}$
Word-line driver:
Charge and discharge the word-line capacitance $C_{Wj}$. 

NMOS transistor $Q_i$:
All output-driving current. 
Charge the bit-line capacitance $C_{Di}$.

"Source follower implementation" OR ROM
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ROM (Read Only Memory)

ROM Cell

MOSFET-based ROM Cell

Active cell device

Word-line driver:
Charge and discharge the word-line capacitance $C_{Wj}$.

NMOS transistor $Q_i$:
Discharge the bit-line capacitance $C_{Di}$.
Good isolation between word and bit line.

"Pull-down device implementation" $\rightarrow$ NOR ROM
Default value of the output is 1
ROM (Read Only Memory)

ROM Cell

$2^m$ multiple-emitter transistors if linear addressing is used.

BJT-based ROM Cell

Used in early bipolar ROMs

Mask programmable connections

Multiple Emitter Transistor

OR ROM
Only one mask layer, the contact mask, is used to program the memory array.

**NOR ROM** The presence of a metal contact to the bit line creates a 0-cell, while its absence indicates a 1-cell.

**Threshold programming**

**NOR ROM** The threshold \( V_{TO} \) of the transistor (1-cell) is selectively raised to a value higher than the voltage swing of the word line \( W_j \).

\( V_{TO} = 7V \) for 5V supply voltage
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ROM (Read Only Memory)

One-dimensional addressing

m-bit address

\[ W_0 \quad W_1 \quad \cdots \quad W_{M-2} \quad W_{M-1} \]

memory matrix

8-bit data

\[ D_7 \quad D_6 \quad D_1 \quad D_0 \]

An example of one-dimensional addressing

Aspect ratio of the memory is not close to the unity.

The shape of storage array is unacceptable.

Problems

Solution is 2-dimensional addressing

Aspect ratio of the memory is close to the unity. Smaller decoders.

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ROM (Read Only Memory)

Two-dimensional addressing

- The number of word lines: $2^m - K$
- Bit line
- Storage Cell
- Word line
- Column decoder
- Column decoder
- Sense Amps/Drivers
- N Output bits: $D_{N-1} - D_0$

An example of 2048 bit ROM (512x4 organization)

- The number of word lines: $2^6 = 64$
- Row decoder
- 2k-bit memory
- 64 X 32 matrix
- The number of bit lines: $4 \cdot 2^3 = 4 \cdot 8 = 32$
- Four 8X1 Multiplexers
- 4 Output bits
- $D_3$, $D_2$, $D_1$, $D_0$
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ROM (Read Only Memory)

Word Expansion

Two 512 X 4-bit ROM

One 512 X 8-bit ROM
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ROM (Read Only Memory)

Address Expansion

2-to-4 decoder

"Glue logic"

2kX4-bit Address space

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ROM (Read Only Memory)

Applications

- Look-up Tables
- Sequence Generators
- Waveform Generators
- Character Generators
- Stored Programs
- Combinational Logic
Nonvolatile Read-Write Memories

Programmable ROMS (PROMS)

Write Once device: OTP ROM (One Time Programmable)

PROM Cell structure allows the customer to program the memory one time.

This is most often accomplished by introducing fuses in the memory cell. (nichrome, polysilicon, or other conductors)

UV EPROM (NVRW memory) without erasing window. Cheap plastic package.
The memory core consists of an array of modified transistors which are programmed by selectively disabling or enabling some of them.

The threshold of the transistor is altered electrically.

The memory must be erased before next programming round.

The Floating-Gate Transistor
The structure is similar to a traditional MOS device, except that an extra polysilicon strip is inserted between the gate and channel.

Electrons are trapped on the floating gate. It results in higher $V_{TO}$

Device cross-section of the FAMOS

Erasing

UV light

Schematic Symbol
**Nonvolatile Read-Write Memories**

**Erasable-Programmable ROM (EPROM)**

EPROM is erased by shining ultraviolet light on the Cells through the transparent window in the package.

**UV-EPROM**

Typical programming time: $5 - 10 \, \mu s / \text{word}$

Erase/Write cycles is generally limited to a maximum of one thousand. Mainly because of UV erasing.

"Off-system" erasure procedure.

Erasing takes time typically up to 1 hour.

Ceramic Packages

The example UV-EPROM chip
Electrically-Erasable-Programmable ROM (EEPROM, E2PROM)

The number of Erasing and Programming cycle is limited

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Read-Write Memories

Introduction

Memory access time
Read and Write time: Independent of memory location.

Memory cycle time
Minimum interval of time required between successive memory operations.

Static RAM
Static memory cell
Basic Storage Cells
NMOS
CMOS

Dynamic RAM
Dynamic memory cell
Needs refreshing

Volatile ↔ Nonvolatile
Local Power Supply
Inside the package

Large dimensions
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**Read-Write Memories**

**Static RAM Cell**

**Assumption:** Linear selection

**Write Operation:**
- Write Data In: 0 1
- Write Enable: 
- X Address: 
- S: 
- R: 
- Q: 0 1
- Read Data Out: 0 1

**Read Operation:** Set X Address to 1.
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Read-Write Memories

Static RAM Cell

Linear selection

m x 1 organized RAM
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Static RAM Cell

NMOS NOR gates

CMOS NOR gates

+ \( V_{DD} \)
A static CMOS memory cell

To R/W=0 of all cells in column j

To R/W=1 of all cells in column j

The 6-MOS Memory Cell

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Read-Write Memories

Static RAM Cell
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Static RAM Cell

2-dimensional addressing of RAM Cell

7-to-128 row decoder

A0-A6

7-to-128 column decoder

X₀

X₁

X₁₂₇

Y₀

Y₁

Y₁₂₇

0-bit line for column 1

1-bit line for column 1

To R/W 0 amplifiers

To R/W 1 amplifiers

1-bit line for column 1

0-bit line for column 1

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Read-Write Memories

Static RAM Cell

2-dimensional addressing of RAM Cell

Storage Cell (1-1) containing 6 NMOS transistors

Millman fig. 9-12
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Static RAM Cell

Cell contains a bit 1

**Assumption:**

*Cell contains a bit 1*

- $Q_2$: Conducts (ON)
- $Q_1$: (OFF)

$V_{N1} \approx V_{DD}$ and $V_{N2} \approx 0V$
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Read-Write Memories

Static RAM Cell

Assumption:

Cell contains a bit 0

- $Q_2$ (OFF)
- $Q_1$ Conducts (ON)

$V_{N2} \approx V_{DD}$ and $V_{N1} \approx 0V$

Cell contains a bit 0
READ CYCLE \[ X_1 = Y_1 = 1 \]

\[ WE = 0 \]

\[ Q_{17} \text{ (OFF)} \]

\[ Write0 = Write1 = \text{don't care} \]

Due to the current through \( Q_8 \) and \( Q_4 \), the voltage drop over \( Q_{12} \) is practically \( V_{DD} \).

\[ V_{GS14} \approx 0V \]

\[ Q_{14} \text{ (OFF)} \implies S = 1 \]
WRITE CYCLE \[ X_1 = Y_1 = 1 \]

\[ WE = 1 \text{ and } W = 1, \bar{W} = 0 \]

\[ Q_{17} \; Q_{10} \; Q_8 \; Q_6 \; (Q_7 \; Q_5) \; (ON) \]

\[ V_{N2} \approx 0V \Rightarrow Q_1 = OFF \]

\[ V_{N1} \approx V_{DD} \]

End of WR-cycle \[ X_1 = Y_1 = 0 \]

\[ WE = 0 \]

\[ Q_5 \; Q_6 \; Q_7 \; Q_8 \; (OFF) \]

\[ Q_1 = OFF \; Q_2 = ON \]

Cell=1
**Dynamic RAM Cell**

**WRITE CYCLE**  
\[ X_i = Y_j = V(I) \]

Write amplifier set the level of the data bit line

Data bit line: \[ V(I) \Rightarrow V_{C1} = V(I) \]

Data bit line: \[ V(0) \Rightarrow V_{C1} = V(0) \]

**READ CYCLE**  
\[ X_i = Y_j = V(I) \]

The read amplifier (sense amp.) detects the voltage level of the data bit line:

\[ C_2 \gg C_1 \Rightarrow V \ll V_1 \]

\[ V = \frac{C_1}{C_1 + C_2} V_{C1} \]

Where \( C_2 \) is capacitance of the data bit line

Read cycle destroys the content of memory cell  
Write original content back

Leakage current  
Refresh time  
ms

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The End